Cache Coherence in eSESC

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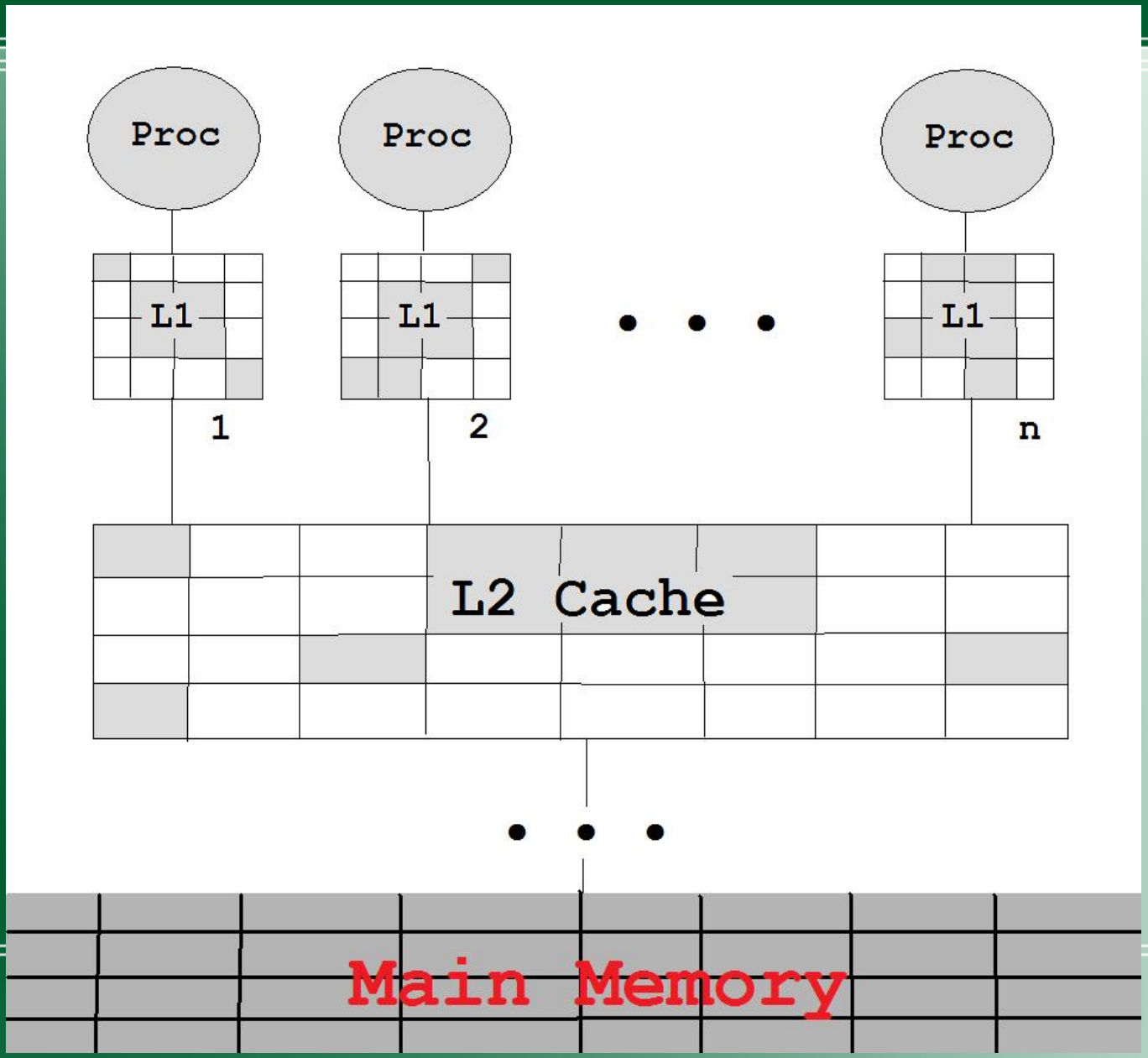
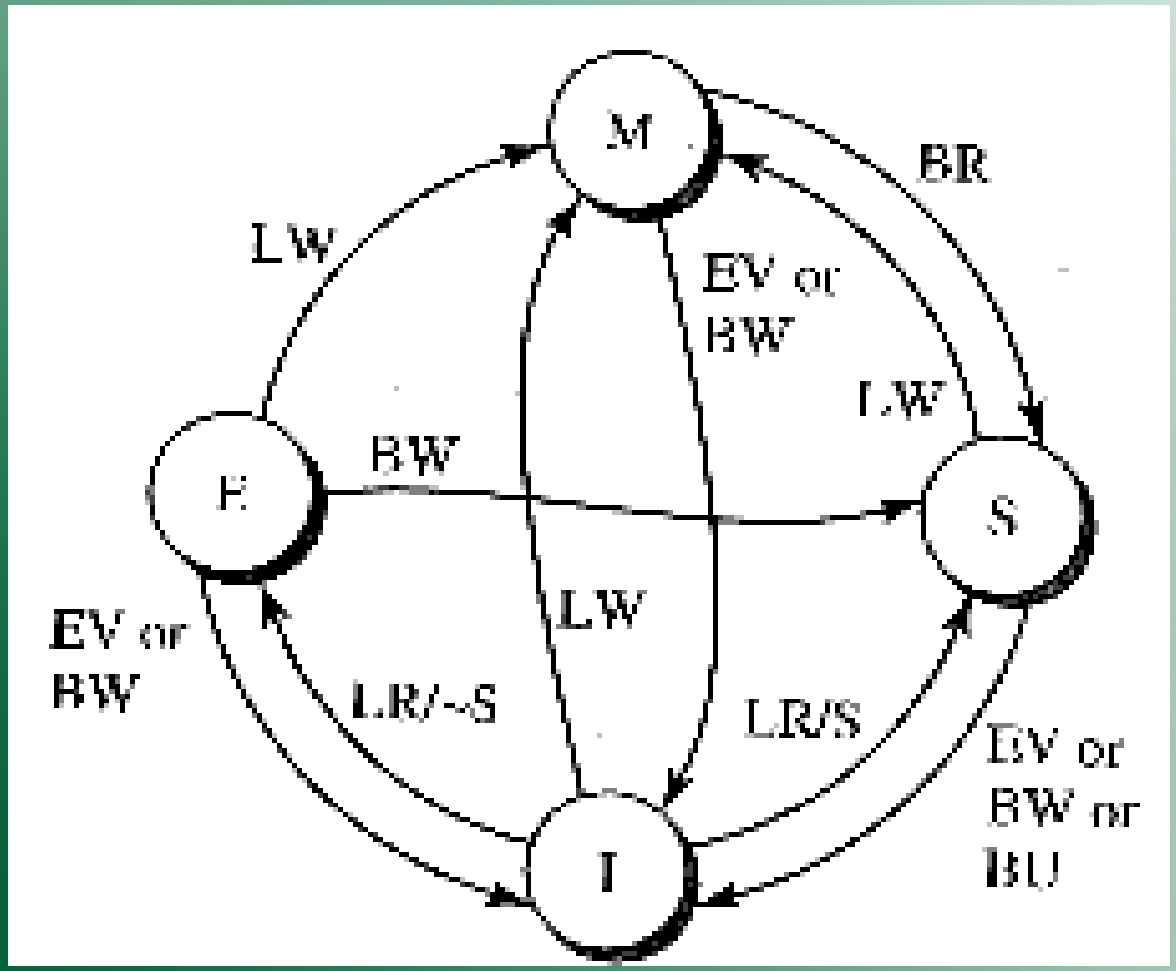
High Level View



High Level View

- L1 Cache
  - Writethrough
  - Allocate on load
  - No-allocate on store
  - MESI protocol
    - Modified,
    - Exclusive
    - Shared
    - Invalid
- L2 Cache
  - Writeback
  - Shared
  - Generates coherence messages
  - Uses directory structure
  - V1: Direct mapped (1-way SA)
  - V2: 2-way SA

Don't mess with MESI (Protocol)



(1)

Code

- Used Cache.cpp as a model
- Added tracking structure for cache line states
  - Multidimensional array
    - Number of cache lines
    - Number of upstream caches
    - Number of ways of associativity
  - Tracking structure

```
typedef struct CacheEntry {
    AddrType Addr;   int State;
}CacheEntryBase;
```

Results

- V2: 2-way associative
- Used default RST input file

```
Proc  Cache Occ MissRate (RD, WR) %DMemAcc MB/s : ...
  0     DL1    0.0   3.57% ( 3.6%, 0.0%) 100.00%  1.13GB/s :
        L2     0.0  100.00% (100.0%, 0.0%)  3.57%  1.13GB/s :  MemBus 0 MB/s :
```

- Same results!

References

- [1]*Modern Processor Design*, J.P. Shen, M. Lipasti, McGraw Hill, New York, 2005.
- [2]*Computer Architecture: A Quantitative Approach*, 4th Ed, J. Hennessy, D. Patterson, Morgan Kaufmann, San Francisco, 2007.
- [3]*The Cache Memory Book*, Jim Handy, Academic Press, San Diego, 1998.